

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Leonard Forbes

Title: DRAM CELLS WITH REPRESSED FLOATING GATE MEMORY, LOW TUNNEL  
BARRIER INTERPOLY INSULATORS

Docket No.: 1303.019US2  
Filed: February 20, 2004  
Examiner: Bradley K Smith

Serial No.: 10/783,695  
Due Date: N/A  
Group Art Unit: 2891

**MS Amendment**


Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

We are transmitting herewith the following attached items (as indicated with an "X"):

- ☒ Communication Concerning Related Applications (1 pg.).  
☒ Supplemental Information Disclosure Statement (2 pgs.), Form 1449 (1 pg.).

If not provided for in a separate paper filed herewith, Please consider this a PETITION FOR EXTENSION OF TIME for sufficient number of months to enter these papers and please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.  
Customer Number 21186

By:   
Atty: David R. Cochran  
Reg. No. 46,632

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being filed using the USPTO's electronic filing system EFS-Web, and is addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 25<sup>th</sup> day of July, 2006.

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SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.  
(GENERAL)

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Applicant:	Leonard Forbes	Examiner: Bradley K. Smith
Serial No.:	10/783,695	Group Art Unit: 2891
Filed:	February 20, 2004	Docket: 1303.019US2
Title:	DRAM CELLS WITH REPRESSED FLOATING GATE MEMORY, LOW TUNNEL BARRIER INTERPOLY INSULATORS	

COMMUNICATION CONCERNING RELATED APPLICATION(S)**MS Amendment**

Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

Applicant would like to bring to the Examiner's attention the following related application(s) in the above-identified patent application:

<u>Serial/Patent No.</u>	<u>Filing Date/Issue Date</u>	<u>Attorney Docket</u>	<u>Title</u>
11471008	June 20, 2006	1303.035US3	PROGRAMMABLE ARRAY LOGIC OR MEMORY WITH P-CHANNEL DEVICES AND ASYMMETRICAL TUNNEL BARRIERS
11471007	June 20, 2006	1303.035US4	PROGRAMMABLE ARRAY LOGIC OR MEMORY WITH P-CHANNEL DEVICES AND ASYMMETRICAL TUNNEL BARRIERS
11471348	June 20, 2006	1303.035US5	PROGRAMMABLE ARRAY LOGIC OR MEMORY WITH P-CHANNEL DEVICES AND ASYMMETRICAL TUNNEL BARRIERS

Continuations and divisionals may be later filed on the cases listed above, or cited to the Examiner in any previous Communication Concerning Related Applications. Applicants request that the Examiner review all continuations and divisionals of the above-listed or previously-cited patent applications before allowing the claims of the present patent application.

Respectfully submitted,

LEONARD FORBES

By Applicant's Representatives,

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Date

25 July 2006

By

  
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